CHARGES CIRCUIT READING BY CALIBRATION AND
CHARGE READING PROCEDURE BY CALIBRATION

5   Technical field and previous technique

The invention concerns a charges circuit reading as well as a charges reading procedure.

More particularly, the invention concerns a charges reading device derived from the detection of
10 radiation by a matrix of N x M elementary detectors as well as a charges reading procedure implemented by such a reading device.

The radiation detected can be, for example, infrared, visible or X rays wavelength radiation. The
15 reading of a detector circuit put together in the form of a matrix of N lines by M columns of elementary detectors is done by scanning, line by line or column by column.

Figure 1 represents a radiation detection device
20 according to the previous article.

The detection device includes N x M ij elementary detectors (I=1, …, N; j=1, …, M), N x M Pj elementary points, M BCj bus column, M Aj charges amplifiers and a MX multiplexing circuit. Each Pij elementary point
25 includes a Tp transistor to adapt the impedance of the ij elementary detector to the reading circuit, a Tc integration transistor and an addressing Ta transistor.

The ij detector is, for example, an N type photovoltaic detector on P substrate. The Tp transistor
30 is a NMOS transistor mounted on a common grid and whose source and drain are respectively connected to the

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detector and to the source of the Tc integration NMOS transistor.

This type pf circuit reading architecture is commonly designated by SCA type architecture (SCA = "Snapshot Charge Amplifier").

A HP clock signal applied to the grid of all the Tp transistors defines the shot time.

The integration function is here implemented by Tc NMOS transistor whose source and drain are linked on the one hand to the Tp transistor drain and on the other hand to the Ta addressing NMOS transistor entry diode. In some cases the source and the Tc drain can be short-circuited.

The same Hci clock signal (I=1, …, N) is applied on the grid of all the Tc transistors on one line. Each line of the circuit reading is attacked by a different Hci signal clock.

The Ta addressing NMOS transistor is mounted on a switch between the drain of the Tc transistor and the connection to the Bcj bus column.

The same Hai clock signal (I=1, …, N) is applied on the grid of Ta transistors of the same line. Each circuit reading line is attacked by a different Hai clock signal.

The Aj charges amplifier (j=1, …, M) contains an AC differential amplifier, a Ca condenser and a Tr transistor.

The BCj bus column links the Pij elementary point exit of the same column to the reverse entry of the AC differential amplifier whose non-reverse entry is linked to a Vref supply.

The Ca capacity and the Tr transistor are mounted in parallel between the reverse entry and the exit of the AC differential amplifier. The Tr transistor is used as a switch to reinitialise the Ca capacity between the readings of two consecutive lines. The Tr transistor grid is guided by a HR clock signal. A Vj voltage is gathered at the exit of the AC differential amplifier.

The charges packet of the Pij elementary points of the same row I line are simultaneously converted in voltage by all the Aj charges amplifiers placed at the edge of the bus columns.

The Vj voltages gathered at the exit of the charges amplifiers are applied on the different entries of a multiplexer in MX voltage to M entries and an exit. The Vs voltage gathered at the exit of the MX multiplexer thus takes as a value the successive values of Vj voltages (j=1, …, M).

When charges-voltage conversion relating to a line of detectors has been made the charges amplifiers are reinitialised so as to enable the charges-voltage conversion of the following line.

An inconvenient factor of a structure such as the one described above is that it generates a high level of noise.

Where there is white noise, the present charges amplifier, with frequencies located in its transmission band, has an amplification factor relating to its intrinsic noise voltage that is given by the following formula:

$$G = ((Cin + Ca) / Ca) \; ½ \quad where$$

Cin is a parasite capacity brought to the reverse entry
of the charges amplifier and Ca is the conversion
capacity of the charges/voltage conversion amplifier.

5   The Cin parasite capacity is proportional to the
number of lines of the matrix of detectors as well as
to the step that separates two detectors of the same
line and the Ca capacity is linked to the maximum
charge that can be integrated in an elementary point.

10   In addition the functioning current of the charges
amplifiers is limited by the consumption imposed on the
circuit.

It follows that the noise level of the reading
circuit is a function of parameters imposed by the

15   technical specifications. This is particularly the case
with highly complex components (for example containing
640 x 480 elementary points) for which the power
dissipated by the charges amplifiers is one of the main
sources of consumption. It is therefore not possible,

20   according to the known technique to produce large
format reading devices that have good noise
performance.

It thus appears that the highly complex SCA type
architectures are limited in noise performance. These

25   limitations are, in addition, amplified for
applications that have a high scene dynamic to process
as is indicated below as an example for a quantal image
sensor produced from hybrid HgCdTe photodiodes on
a CMOS circuit and meeting the following technical

30   specifications:

   - maximum photonic current:

$$Imax = 2Na$$
$$Ph$$

- duration of the image shot:

$$Ti = 1mS$$

- equivalent rms noise voltage brought to entry of the charges amplifier:

$$ea = 80\mu \text{ V rms}$$

- parasite capacity of bus column (parasite capacity view on reverse entry of the amplifier):

$$Cin = 4pF$$

- maximum exit excursion of the charges amplifier:

$$vsmax = 2V$$

For such an image sensor the maximum charge that it is possible to store in an elementary image point is:

$$Q \text{ Max} = IMax \text{ } xTi = 2pC$$
$$PEL \quad ph$$

The capacity of the charges-voltage conversion condenser of the charges amplifier can be written as follows:

$$C_a = \frac{Q_{PEL}^{Max}}{\Delta Vs^{Max}} = 1pF$$

The es equivalent noise at the exit of the charges amplifier is written as follows:

$$Es = G \times ea$$

Where G is the amplification factor mentioned above.

The following thus applies:

$$Es \quad 180\mu \text{ V rms}$$

Generally in quantal sensors the processing chain degrading by a 2 factor the noise performances of detectors under minimum flux is tolerated. That

means that the noise associated with the reading
circuit is at the most equal to the noise associated
with the detector under minimum lighting conditions.

Where there are photovoltaic detectors that
5   only have a Schottky noise source the following
applies:

$$e_s = \sqrt{\frac{I_{ph}^{min} \times Ti}{q}} \times \frac{q}{c_a}$$

Where Imin is the minimum detectable photonic current

10 Therefore:

$$I_{ph}^{min} = \frac{(e_s \times c_a)^2}{q \times Ti}$$

Ie here:

$$I_{ph}^{min} = 200pA.$$

The maximum dynamic of intensity that the reading
15 circuit is capable of processing is thus:

$$D = \frac{I_{ph}^{Max}}{I_{ph}^{min}} \# 10$$

In   certain   applications   this   dynamic   is   not
sufficient. For very varied scenes for example, a
dynamic of 100 may be necessary.
20   In addition according to current technique the
Volt/coulomb response of the reading circuit is the
same for all the elementary points. This response is
therefore a weak value for elementary points whose
detected charge has a weak quantity. This is the case
25 particularly for images under reduced   incident flux
when it is not possible to increase the integration
time   (image   rate   problem   and/   or   moved   during

shooting). This is also the case when the imaged scene presents a significant contrast: detected charge near saturation for certain photodiodes and much lower than saturation for others. A weak value response in
5 Volt/Coulomb is manifested by a greater sensitivity relative to the shift of the quiescent point of the multiplexing chain (column exit to video exit) and a lesser immunity to noises (stray coupling) on the video signal.

10 The invention does not present the drawbacks mentioned above.

Indeed the invention concerns a charges reading circuit containing charges storage material, charges addressing material and charges/voltage conversion
15 including a capacity conversion, addressing material enabling injection control, in the conversion material, charges stored in the storage equipment. The circuit contains calibration material to deliver representative information of the stored charges in the storage
20 material and material for selecting the conversion capacity from the said information.

The invention also concerns a reading device for charges derived from the detection of radiation by a matrix of N lines by M columns of elementary detectors,
25 reading device including a total of N x M elementary points and charges/voltage conversion material, each elementary point being linked to an elementary detector and including storage material to store the charges detected by the elementary detector to which it is
30 linked and addressing material to control the injection in the conversion material, charges stored in the

storage material, the conversion material containing a conversion capacity. The device is characterised by the fact that an elementary point includes calibration storage material to stock a fraction of the stored

5   charges in storage material and at least one addressing material to control the injection in the conversion equipment, stored charges in the calibration storage material and in the fact that the conversion material includes a first calibration capacity to convert the

10 addressed charges coming from the calibration storage material in a calibration voltage and material to select the conversion capacity from the calibration voltage.

      The invention also concerns a charges reading

15 process including successively a charges storage stage, a charges addressing stage and a charges/voltage conversion stage, the addressing stage enabling control of the injection in charges/voltage conversion equipment including a conversion capacity, charges

20 stored during the storage stage. The process includes a calibration stage to deliver information representative of the stored charges during the storage stage and a selection stage of the conversion capacity from the said information.

25   The invention also concerns a reading process for charges derived from the detection of radiation by a matrix of N lines by M columns of elementary detectors, the process including a reading stage of charges detected by each elementary detector. The reading stage

30 of the charges detected by each elementary detector is

done by a reading process like the process according to the invention mentioned above.

Brief description of the figures

5   Other characteristics and advantages of the invention will appear on reading a preferential mode of production of the invention done in reference to the appended figures among which:

- figure 1 represents a SCA type charges reading
10   device according to the previous kind
- figure 2 represents an SCA type charges reading device according to the invention
- figure 3 represents a perfecting if the SCA type charges reading device according to the invention
15

Detailed description of the implementation mode of the invention

Figure 1 has been previously described. There is therefore no point returning to it.

20   Figure 2 represents a charges reading device according to the invention. For reasons of simplicity only an elementary detector made up of a ij diode and a Pij elementary point, a BCj bus column and a Aj charge amplifier are represented on figure 2.

25   Generally, the invention nevertheless concerns a reading device structured in the form of a matrix containing M x N elementary detectors.

An elementary point according to the invention includes as well as the Tp, Tc and Ta transistors at

30   least one extra circuit mounted in parallel to the Tc

and Ta transistors and made up of a Il switch and two extra Tccal and Tacal transistors.

A charges amplifier according to the invention includes a K comparer, an AC differential amplifier, a Ccal conversion capacity mounted between the exit and reverse entry of the AC differential amplifier and at least one extra circuit mounted in parallel to the Ccal capacity and made up of a I2 switch and C supplementary conversion capacity. A Tr transistor whose grid is guided by HR clock signal is used as a switch to reinitialise the integration capacity.

As a non-limiting example the elementary point illustrated in figure 2 only contains a single supplementary circuit mounted in parallel to the Tc and Ta transistors and the charges amplifier only includes a single supplementary circuit mounted in parallel with the Ccal capacity.

When the Il switch is closed the photonic current delivered by the ij diode attacks the channel of the two Tc and Tccal MOS integration transistors. The Il switch enables control of the integration in the Tccal transistor. It prevents the stored charges returning into the TC cal transistor during the elementary point reading. The Ta and Tacal transistors enable control of the injection of the stored charges respectively in the Tc and TC cal transistors according to the SCA principle.

The BCj bus column attacks the reverse entry of the Aj charges amplifier whose non-reverse entry is linked to a Vref reference voltage. The C condenser is connected in parallel of the Ccal connector through the

I2 switch. The I2 switch is controlled by a Slog logical comparison signal derived from the K comparator. The Slog signal is issued from the comparison of the Vs tapping in exit of the AC

5   differential amplifier with a Vthreshold threshold voltage.

The shot is done by simultaneous integration of the detected charges in the Tc and Tccal transistors (the I1 switch is in closed position). The integration

10   capacity of the Pij elementary point is then the total of the integration capacity presented by the Tc transistor and the integration capacity presented by the Tccal transistor.

Once the shot has been taken the charges reading

15   stored in the elementary point is carried out according to two successive phases.

In a first phase the I2 switch is open, only the Qcal charge stored in the TC cal transistor is injected in the C cal conversion capacity of the Aij amplifier,

20   reinitialised beforehand by Tr. Hccali   and Hccali clock signals are then applied on the grids of respectively the Tacal and TC cal transistors to authorize the transfer of the Qcal charges. The ΔV_{conv}^{max} variation of the Vs exit of the Aj amplifier is

25   then given by the formula:

$$\Delta V_{conv}^{max} = Q_{cal}/C_{cal}.$$

This voltage variation constitutes a representative measure of the total charge stored in the elementary point. If the voltage variation

30   ΔV_{conv}^{max} carries the Vs voltage to a value higher than the

threshold tension Vthreshold, the K comparator delivers
a Slog comparison logical signal that controls the
closing of the I2 switch. The reverse reaction capacity
of the Aj amplifier is then made up of C and Ccal
5 condensers in parallel. In the opposite event the I2
switch is not closed again and only the Ccal condenser
remains connected in a reverse reaction.

In a second phase the Hai clock signal applied on
the Ta transistor grille authorises the transfer of the
10 stored charges in the TC transistor to the reverse
reaction capacity of the Aj amplifier. The charge
stored in the Tc transistor is then transferred either
to the Ccal capacity only or to the Ccal and C
capacities in parallel.

15 The information available in output of the Aj
amplifier is made up of the Vs conversion voltage
delivered by the AC differential amplifier and the Slog
comparison signal delivered by the K comparator. The Vs
signal alone does not allow the value of the stored
20 charge to be recovered. To recover the value of the
stored charge the calibre that was used to make the
measurement must be known. This calibre is given by the
Slog comparison signal. The value of the stored charge
is then calculated from the Vs conversion voltage and
25 the Slog comparison signal.

Indeed for the same Vs value you can go back to
two charge values (one stored on Ccal the other on
Ccal and C) for very different values. This reading
mode is applied, line by line, to all the elementary
30 points of the column.

According to the mode of production of the invention described above, two conversion calibres are used for the charges/voltage conversion. In a more general way the invention concerns a charge reading device including at least P conversion calibre, P being a number higher than or equal to 2. The K comparator then works on P-1 levels.

An example of production of reading circuit according to the invention will now be described. The reading circuit includes:

- a Tc integration transistor whose value of the integration capacity is equal to $9 \times Cint/10$
- a Tcal supplementary integration transistor whose value of integration capacity is equal to $Cint/10$
- a Ccal capacity whose value is equal to $Cref/10$ and
- a C capacity whose capacity value is equal to $9 \times Cref/10$

since the value of Cref is a reference capacity value for example equal to 1pF and Cint is the same order of magnitude.

When the I1 switch is closed the total integration capacity therefore has Cint as a value. Likewise when the I2 switch is closed the total conversion capacity has Cref as a value.

Let us suppose that the maximum voltage variation at the edges of the total reading capacity is equal to 1 volt and the threshold voltage of the comparator is equal to 0.1 volt.

If the photo-charge integrated in a elementary point develops a voltage variation less than 0.1 volt

then the exit voltage of the Aj charge amplifier is equally less than 0.1 volt at the end of the first phase. The I2 switch remains open and the charge stored in the Tc integration transistor is transmitted in the Ccal capacity. The conversion in voltage is thus carried out on a capacitive calibre with a value of Cref/10.

If the photo-charge integrated in an elementary point develops a voltage variation higher than 0.1 volt then the exit of the Aj charge amplifier is also higher than 0.1 volt at the end of the first phase. The I2 switch closes and the charge stored in the Tc integration transistor is transmitted in the Ccal + C capacity. The conversion in voltage is thus made on a capacitive calibre with a value of Cref.

To sum up, if the integrated charge is lower than Cint x 0.1 V the response of the Aj amplifier is equal to [Cref/10]-1 Volt/Coulomb and, if the integrated charge is higher than Cint x 0.1 V, the response of the Aj amplifier is equal to Cref-1 Volt/Coulomb.

Between the two conversion phases, the charges amplifier can be reinitialised or not, a reinitialisation of the charges amplifier leading to a loss of the Qcal charge.

The presence of a calibre with high-level conversion sensitivity ([Cref/10]-1 Volt/Coulomb) enables the favourable processing of the detection of weak quantities of charges corresponding to a weak photonic current, for example a Iph current less than 200pA.

Where the calibre of a high-level conversion sensitivity is used, the noise amplification factor in exit of the charges amplifier is written:

$$G = ((Cin + Ccal)/Ccal)^{\frac{1}{2}}$$

5   All things equal also (see the digital example above), the ea noise equivalent in exit of the charges amplifier is thus written:

$$Es = 510 \quad Vrms$$

To good effect, it seems thus that the signal is 10 increased by a factor of 10 [(C+Ccal)/Ccal] while the process chain noise only increases by a factor of 2.8 (510/180).

In the event of photovoltaic detector with only a Schottky noise source, the dynamic limitation that it 15 is possible to process with the high sensitivity calibre is indicated by the following equation:

$$I_{ph}^{min} = \frac{(e_s \times Ccal)^2}{q \times Ti} \qquad (3)$$

It then comes to:

$$I_{ph}^{min} = 8pA$$

20   The maximum dynamic that the reading circuit can process is thus written:

$$D = \frac{I_{ph}^{Max}}{I_{ph}^{min}} \#120$$

The high sensitivity calibre thus enables a considerable increase of the processing dynamic of a 25 SCA type architecture.

As shown in figure 3 according to a perfecting of the invention the Slog logical signal generated during the calibration phase and used to select the calibre of charges/voltage conversion can also be used to adjust

the quiescent current of the charges amplifier according to the charges packet to be converted. The reading circuit according to the invention thus includes Mj adjusting material of the quiescent current

5   controlled by the Slog comparison logical signal.

This enables optimisation of the consumption of charges amplifiers of the reading device according to the quantity of charges to be converted.

If the quiescent current of the charges amplifier

10   is fixed at a I1 value where the Vs measured during the calibration phase is lower than the Vthreshold voltage it is then possible to bring the quiescent current to a I2 value higher than I1 where the Vs voltage measured during the calibration phase is higher than Vthreshold.